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contd

layer of the array stack. However, the inventor believes it to be more useful and necessary the closer such level is to the top layer, wherein reduction of physical distortion is most critical, although the inventor acknowledges that other authorities have proposed that such correction is most critical in the lower levels.

IN THE CLAIMS

Please delete claim 5.

Please amend Claims 1, 6 and 7 as shown in the attached "Version With Markings To Show Changes Made," to read as follows:

subC7
AS
1. (Amended) A method for creating a dummy metal fill pattern near functional circuitry, comprising:

- a. creating a margin area around the functional circuitry;
 - b. trimming a dummy fill pattern to the margin area to create a trimmed fill pattern; and
 - c. overlaying said trimmed fill pattern and the functional circuitry; and
- wherein the dummy fill pattern is an example of an alternative functional circuitry.

6. (Amended) The method for creating a dummy metal fill pattern of claim 1, wherein:
the alternative functional circuitry is selected to be alike to that near the functional circuitry.

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7. (Amended) The method for creating a dummy metal fill pattern of claim 1, wherein:
the alternative functional circuitry is a selected portion of functional circuitry from a metal layer on which the dummy metal fill pattern is to be used.

REMARKS

These remarks are in response to the Office Action dated December 18, 2002, which has a shortened statutory period for response set to expire March 18, 2003. A one-month extension, to expire April 18, 2003, is requested in a petition filed herewith.